Raspberry Pi Compute Module Zero

A Raspberry Pi for deeply embedded applications

Colophon

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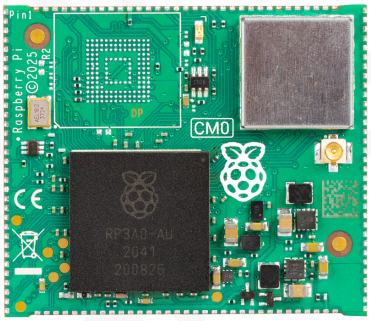
1. Introduction

Compute Module Zero (CM0) is a System on Module (SoM) built around the RP3A0 chip, a custom-built system-in-package designed by Raspberry Pi. It provides the core processing capability of Raspberry Pi Zero 2 W in a compact, embeddable form factor, with onboard RAM and optional Wi-Fi connectivity. It enables developers and system designers to add Raspberry Pi functionality to custom hardware designs.

Figure 1.
The front of Compute Module Zero (CM0)



The CM0 module is designed to be soldered directly onto the carrier board. The CM0 provides 132 castellated connections arranged around the edge of the module, spaced at a 1 mm pitch. You can solder the module manually or using standard surface-mount processes during automated PCB assembly.

1.1. Features

CM0 is based on Raspberry Pi Zero 2 W. This means that you can test your projects on Raspberry Pi Zero 2 W before building the final CM0-based product.

CM0 is also available without the eMMC storage; this variant is called Compute Module Zero Lite (CM0Lite). Unless otherwise stated, within this document, CM0 also refers to CM0Lite.

Key features of CM0 are as follows:

- **High-performance SoC.** Broadcom BCM2837 quad-core Cortex-A53 (Armv8) 64-bit processor running at 1 GHz.
- **Compact module design.** Small footprint of 39 mm × 33 mm × 2.8 mm.
- **Video support.** Can decode and encode videos at Full HD (1080p) and 30 frames per second.
  - Decode (1080p30) in H.264 or MPEG-4.
  - Encode (1080p30) in H.264.
- **Graphics support.** Supports 2D and 3D graphics using OpenGL ES 1.1 and 2.0.
- **Memory (RAM).** 512 MB of LPDDR2 memory.
- **Optional flash storage.** Optional onboard eMMC in 8 GB or 16 GB.
- **Additional SDIO interface for CM0Lite.** External storage or peripheral expansion in place of onboard eMMC (CM0Lite only).
- **Optional wireless connectivity.** Optional Wi-Fi and Bluetooth with external antenna socket.
- **GPIO.** 28 pins.
- **Camera support.** 4-lane CSI camera interface.
- **Display support.**
  - HDMI.
  - 4-lane Display Serial Interface (DSI).
  - Display Parallel Interface (DPI).
  - Composite video output.
- **Power input.** Single 5 V PSU input.

2. Interfaces

Compute Module Zero includes a range of interfaces to support diverse applications, from storage and networking to wireless communication, display outputs, and flexible GPIO expansion. These interfaces allow you to build connected and adaptable embedded systems. The following sections provide technical information on each available interface, including configuration options, routing guidelines, and design considerations.

2.1. Wireless

CM0 supports both **Wi-Fi** and **Bluetooth** functionality, allowing developers and system designers to flexibly manage wireless connectivity for a range of applications. The wireless interfaces are provided by the **Cypress CYW43459** chip, supporting both:

- 2.4 GHz IEEE 802.11 b/g/n Wi-Fi.
- Bluetooth 5.0 and BLE.

The antenna uses a standard IPEX-1 connector, and Raspberry Pi Ltd provides a certified antenna for use with CM0. If you choose to use a third-party antenna, you must obtain your own certification because Raspberry Pi Ltd doesn't support certification for non-approved antennas.

You can enable and disable wireless functions independently as required. For example, in kiosk deployments, a service engineer might temporarily enable wireless to perform updates, then disable it for security and regulatory compliance.

To support power savings and regulatory requirements, CM0 includes two control pins: `WiFi_ON` and `BT_ON` . These pins are reserved on Compute Modules without wireless functionality to allow hardware-level shut down of Wi-Fi and Bluetooth.

2.1.1. Wi-Fi on (`WiFi_ON`)

The `WiFi_ON` pin indicates the enable/disable state of Wi-Fi and may also be used to disable Wi-Fi. This pin may only be driven low; it can't be driven high. The software driver drives it high internally when required.

- If the pin is high (logic 1), Wi-Fi is powered up. If Wi-Fi is enabled after being disabled, you must reinitialise the Wi-Fi driver.
- When driven or tied low (logic 0), the pin prevents Wi-Fi from powering up, helping to reduce power consumption or meet requirements to physically disable Wi-Fi.

2.1.2. Bluetooth on (`BT_ON`)

The `BT_ON` pin indicates the enable/disable state of Bluetooth and may also be used to disable Bluetooth. This pin may only be driven low; it can't be driven high. The software driver drives it high internally when required.

- If the pin is high (logic 1), Bluetooth is powered up. If Bluetooth is enabled after being disabled, you must reinitialise the Bluetooth driver.
- When driven or tied low (logic 0), the pin prevents Bluetooth from powering up, helping to reduce power consumption or meet requirements to physically disable Bluetooth.

2.2. USB 2.0 (High-Speed) interface

The USB 2.0 interface supports up to 480 Mb/s signalling. The differential pair should be routed with a 90 Ω differential impedance. The P and N signals within each differential pair should be length-matched, ideally within 0.15 mm.

To enable USB 2.0 functionality, add the `dtoverlay=dwc2,dr_mode=host` overlay setting to your `config.txt` file.

Note

The USB 2.0 port can operate in USB On-The-Go (OTG) mode. While not officially documented, some users have successfully enabled this functionality. The `USB_OTG_ID` pin determines the role (host or device) and is typically connected to the ID pin of a Micro USB connector. To use OTG functionality, it must be enabled in the operating system (OS). For fixed-role use, tie the `USB_OTG_ID` pin to ground.

2.3. Camera Serial Interface (CSI)

CM0 supports a 4-lane CSI interface for high-speed camera connections. The interface uses four 100 Ω differential pairs. Within a pair, the signals should be length-matched within 0.15 mm.

The following camera sensors are supported by official Raspberry Pi firmware:

- OmniVision OV5647
- Sony IMX219
- Sony IMX296
- Sony IMX477
- Sony IMX708

For more information about the CSI interface, see Raspberry Pi documentation.

2.4. Video and display interfaces

CM0 supports multiple display interfaces and can drive up to three simultaneous displays of any of the following types:

Table 1.
Video and display interfaces supported by Compute Module Zero (CM0)

Interface	Description
HDMI	High-speed digital differential pair display interface; 1080p30
DSI	High-speed 4-lane differential pair display interface
DPI	Parallel display interface through GPIO
CVBS	Analog composite video interface; requires 75 Ω termination

2.4.1. HDMI

CM0 includes an HDMI interface supporting 1080p30. Consider the following to ensure reliable HDMI operation:

- HDMI signals must be routed as 100 Ω differential pairs.
  - Within a pair, each signal should be length-matched within 0.15 mm.
  - Between pairs, length matching within 25 mm is sufficient.
- Consumer Electronics Control (CEC) is supported, with an internal 27 kΩ pull-up resistor included in CM0.
- Hotplug Detect (HPD) is supported, with an internal 100 kΩ pull-down resistor included in CM0.
- Extended Display Identification Data (EDID) signals have internal pull-up resistors in CM0.
- Like Raspberry Pi 5, CM0 doesn't have extra ESD protection on HDMI signals because it isn't typically required. Consider whether you might need extra ESD protection and then add it if required.

2.4.2. Display Serial Interface (DSI)

CM0 supports connection to DSI-compatible displays through the high-speed digital DSI interface. The DSI interface uses four differential pairs. The signals must be routed as 100 Ω differential pairs. Within a pair, the signals should be length-matched within 0.15 mm.

CM0 is compatible with displays supported either by the:

- Official Raspberry Pi firmware.
- Mainline Linux kernel.

For third-party displays not officially supported, you must provide a custom driver.

2.4.3. Display Parallel Interface (DPI)

CM0 supports up to 24-bit RGB video with 4 control signals: `PCLK` , `DE` , `VSYNC` , and `HSYNC` . The DPI interface replaces GPIO signals. It's possible to use reduce colour depth to retain some GPIO functionality.

2.4.4. Composite video (CVBS)

CM0 can output standard analog video (composite video, also called CVBS) in a range of formats. The `CVBS` signal is designed to drive a 75 Ω mode.

2.5. I2C interfaces

CM0 provides two I2C buses that can be repurposed depending on system configuration and peripheral usage.

2.5.1. CSI/DSI I2C bus (`SDA0` and `SCL0`)

The CSI/DSI I2C bus is normally allocated to the CSI and DSI interfaces. However, it can be used as a general I2C bus or GPIO if not being used by the CSI and DSI interfaces:

- The serial data pin (`SDA0`) is connected to `GPIO44` .
- The serial clock pin (`SCL0`) is connected to `GPIO45` .

2.5.2. HAT EEPROM identification I2C bus (`ID_SD` and `ID_SC`)

The HAT EEPROM identification I2C bus consists of signals on the `ID_SD` (data) and `ID_SC` (clock) pins. This bus is typically reserved for identifying HATs.

If the firmware isn't using this I2C bus (for example, no HAT ID EEPROMs being used), then these pins can be repurposed as `GPIO0` and `GPIO1` if needed. When using these pins as GPIO pins, add `force_eeprom_read=0` to the `config.txt` file. This prevents the firmware from checking whether there's a HAT EEPROM available.

2.6. SDIO (CM0Lite only)

CM0Lite doesn't include onboard eMMC storage. Instead, it provides a **Secure Digital Input Output (SDIO)** interface for connecting external storage devices. To ensure proper signalling, the SDIO interface requires a reference voltage (`SD_VREF`) that matches the type of storage being used.

Table 2.
SDIO storage configuration for CM0Lite

Storage Type	Connection	Reference voltage
External eMMC	SDIO	Connect `SD_VREF` to 1.8 V (`CM0_1.8V`)for 1.8 V signalling
External SD card	SDIO	Connect `SD_VREF` to 3.3 V (`CM0_3.3V`) for 3.3 V signalling
Onboard eMMC	N/A	Not present; `SD_VREF` can be left floating or connected to 1.8 V (`CM0_1.8V`)

2.7. GPIO

There are 28 general-purpose I/O (GPIO) pins available, which correspond to the GPIO pins on the Raspberry Pi 5 40-pin header. These pins have access to internal peripherals, such as SMI, DPI, I2C, PWM, SPI, and UART. Details about these features and the available multiplexing options are the same as described in the BCM2835 ARM peripherals document.

To minimise electromagnetic compatibility (EMC) issues, we recommend setting the drive strength and slew rate to the lowest levels necessary. GPIO2 and GPIO3 include 1.8 kΩ pull-up resistors.

The GPIO bank is powered by the `GPIO_VREF` supply. This can connect to `CM0_1.8V` for 1.8 V signalling or `CM0_3.3V` for 3.3 V signalling. Don't exceed 50 mA for total current load on all 28 GPIO pins. `GPIO_VREF` must be connected to either `CM0_3.3v` or `CM0_1.8v` .

2.7.1. Alternative function assignments

Up to six alternative function assignments are available on the GPIO pins. The following table provides an overview of these alternative functions. For more detailed information about these functions, see the peripherals datasheet.

Each GPIO can have only one function at a time.

Function selections without a named function in the following table are reserved.

Table 3.

GPIO function selection

GPIO	Default Pull	Function					
		ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
0	High	SDA0	SA5	DPI_PCLK			
1	High	SCL0	SA4	DPI_DE			
2	High	SDA1	SA3	DPI_VSYNC			
3	High	SCL1	SA2	DPI_HSYNC			
4	High	GPCLK0	SA1	DPI_D0			ARM_TDI
5	High	GPCLK1	SA0	DPI_D1			ARM_TDO
6	High	GPCLK2	SOE_N	DPI_D2			ARM_RTCK
7	High	SPI0_CSn1	SWE_N	DPI_D3			
8	High	SPI0_CSn0	SD0	DPI_D4			
9	Low	SPI0_MISO	SD1	DPI_D5			
10	Low	SPI0_MOSI	SD2	DPI_D6			
11	Low	SPI0_SCLK	SD3	DPI_D7			
12	Low	PWM0	SD4	DPI_D8			ARM_TMS
13	Low	PWM1	SD5	DPI_D9			ARM_TCK
14	Low	TXD0	SD6	DPI_D10			TXD1
15	Low	RXD0	SD7	DPI_D11			RXD1
16	Low	FL0	SD8	DPI_D12	CTS0	SPI1_CSn2	CTS1
17	Low	FL1	SD9	DPI_D13	RTS0	SPI1_CSn1	RTS1
18	Low	PCM_CLK	SD10	DPI_D14		SPI1_CSn0	PWM0
19	Low	PCM_FS	SD11	DPI_D15		SPI1_MISO	PWM1
20	Low	PCM_DIN	SD12	DPI_D16		SPI1_MOSI	GPCLK0
21	Low	PCM_DOUT	SD13	DPI_D17		SPI1_SCLK	GPCLK1
22	Low	SD0_CLK	SD14	DPI_D18	SD1_CLK	ARM_TRST	
23	Low	SD0_CMD	SD15	DPI_D19	SD1_CMD	ARM_RTCK	
24	Low	SD0_DAT0	SD16	DPI_D20	SD1_DAT0	ARM_TDO	
25	Low	SD0_DAT1	SD17	DPI_D21	SD1_DAT1	ARM_TCK	
26	Low	SD0_DAT2	TE0	DPI_D22	SD1_DAT2	ARM_TDI	
27	Low	SD0_DAT3	TE1	DPI_D23	SD1_DAT3	ARM_TMS	
28	None	SDA0	SA5	PCM_CLK	FL0		
29	None	SCL0	SA4	PCM_FS	FL1		
40	Low	PWM0	SD4		SD1_DAT4	SPI2_MSIO	TXD1
41	Low	PWM1	SD5	TE0	SD1_DAT5	SPI2_MOSI	RXD1
42	Low	GPCLK0	SD6	TE1	SD1_DAT6	SPI2_SCLK	RTS1

GPIO	Default Pull	Function					
44	None	GPCLK1	SDA0	SDA1	TE0	SPI2_CSn1	
45	None	PWM1	SCL0	SCL1	TE1	SPI2_CSn2	

2.7.2. Alternative GPIO functions

A variety of alternative GPIO functions accommodate diverse peripheral interfaces and communication protocols. The following list summarises the available peripherals and their supported configurations:

- Two UARTs, with standard signals (`TXD` , `RXD` , `CTS` , `RTS`).
- One 4-bit SDIO for Secure Digital Input/Output.
- Two PWM channels for pulse-width modulation.
- Three general-purpose clock (GPCLK) outputs.
- One DPI (Display Parallel Interface) with `PCLK` , `DE` , `VSYNC` , `HSYNC` , and up to 24-bit data.
- Two I2C controllers.
- Three SPI controllers.

2.7.3. Camera GPIO (`CAM_GPIO`)

CM0 provides a dedicated GPIO for controlling the camera module, called `CAM_GPIO0` . The `CAM_GPIO0` control signal is typically connected to pin 17 on the camera connector. This signal is used to control power to the camera module. `CAM_GPIO0` corresponds internally to `GPIO40` on the board.

2.8. Status LED (`LED_nACT`)

GPIO29 on the SoC controls the `LED_nACT` pin, which replicates the onboard status LED that shows board activity. The status LED behaves similarly to the green LED on Raspberry Pi Zero 2 W. Under Linux:

- The LED flashes during eMMC or SD card activity.
- If a boot error occurs, the LED flashes in a specific error pattern.

To decode these patterns, see the LED Flash codes in the Raspberry Pi documentation.

The signal is active low and should be buffered if driving an external LED.

2.9. Power management and control

The following signals, summarised in Table 4, relate to power sequencing, boot source selection, and system readiness signalling for CM0: `GLOBAL_EN` , `nRPI_BOOT` , and `RUN_PG` .

Table 4.
System control signals

Pin	Description	Usage
`GLOBAL_EN`	Controls the power-down state of CM0.	Pull low to put CM0 in the lowest power-down state. We recommend only pulling this pin low after OS shutdown.
`nRPI_BOOT`	Determines boot source during startup.	Hold low during boot to bypass eMMC and boot through USB 2.0 instead.
`RUN_PG`	The signal goes high when the PSUs have powered up.	May be driven low to delay powerup or reset the module. We recommend only pulling this pin low after OS shutdown

3. Power

CM0 requires a regulated 5 V supply for operation. CM0 can also supply 600 mA at 3.3 V and 1.8 V to peripherals. The following sections describe the required power-up and power-down sequences, typical and maximum power consumption, and the capabilities of the on-board voltage regulators.

3.1. Power-up sequencing

The following list summarises the power-up conditions and sequencing necessary for proper power-up of CM0:

- No pins should be powered before the 5 V rail is active.
- To boot CM0 through USB, the `nRPI_BOOT` pin must be low within 1 ms after the 5 V rail rises.
- The 5 V rail should rise monotonically to at least 4.75 V and remain above this level during operation.
- The power-up sequence begins after the 5 V rail is above 4.75 V and the `GLOBAL_EN` signal rises.
- The power rails and signals rise in the following order:
    1. 5 V rises
    2. `GLOBAL_EN` rises
    3. `CM0_3.3V` rises
    4. `CM0_1.8V` rises at least 1 ms after `CM0_3.3V`

3.2. Power-down sequencing

The following list summarises the recommended power-down procedure and considerations for CM0 to ensure safe shutdown and file system integrity:

- To ensure file system consistency, shut down the operating system before removing power.
- If controlled shutdown isn't possible, consider using file systems like `btrfs` , `f2fs` , or `overlayfs` , which can be enabled through `raspi-config` .
- After the operating system has shut down, the 5 V rail can be removed or the `GLOBAL_EN` pin can be taken low to put the CM0 into the lowest power mode.
- During the shutdown sequence, `CM0_1.8V` will be discharged before the `CM0_3.3V` rail.

3.3. Power consumption

The exact power consumption of CM0 depends on the tasks being run on it. Typical values are summarised below:

- The lowest shutdown power consumption mode occurs when `GLOBAL_EN` is driven low, typically around 500 µA.
- Idle power consumption is typically 225 mA, but this varies depending on the operating system.
- Operating power consumption is typically around 675 mA, but this depends on the operating system and running tasks.

3.4. Regulator outputs

CM0 has built-in voltage regulators that provide 3.3 V (`CM0_3.3V`) and 1.8 V (`CM0_1.8V`) power rails. These regulators can each deliver up to 600 mA of current to external devices or peripherals connected to the board. The current drawn by connected devices from these regulators isn't included in the overall power consumption figures; the reported power usage only accounts for the board itself, not the extra peripherals powered through these regulators.

4. Specifications

This section includes technical descriptions of CM0's components and capabilities, including its dimensions, pinout, electrical specifications, thermal characteristics, and MTBF calculations.

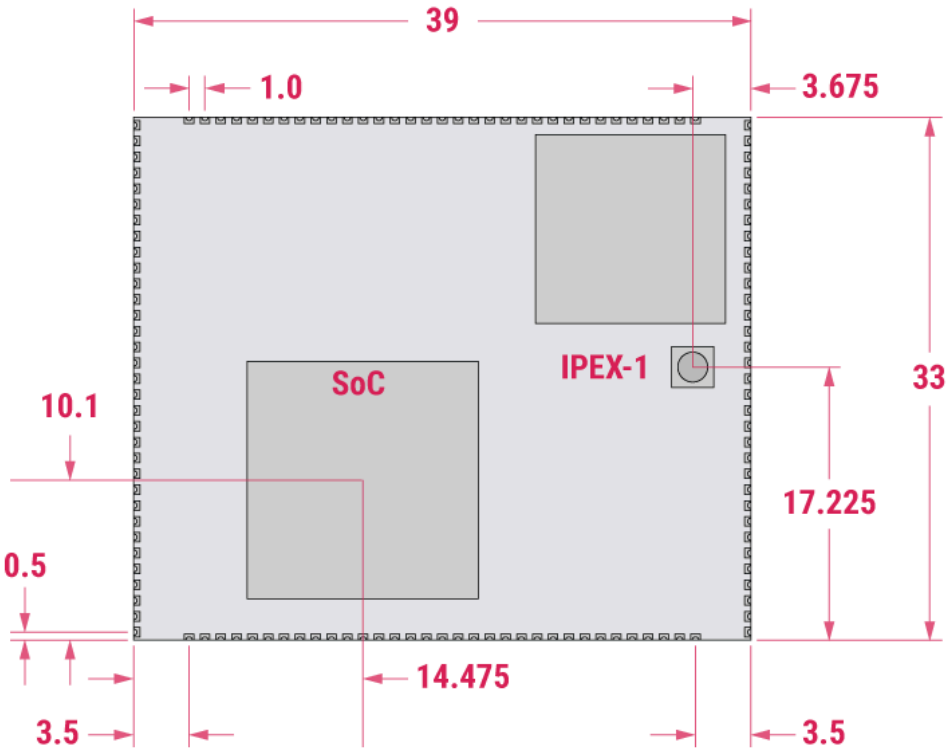
4.1. Mechanical specifications

CM0's consists of a compact PCB made from FR4 material. Its 132 pins are 1 mm-pitch castellations, implemented as plated half-holes with a high-quality nickel/gold (ENIG) finish for reliable soldering. The following sections provide more information about the PCB dimensions and recommended footprint of CM0.

4.1.1. PCB dimensions

CM0 is a compact 39 mm × 33 mm × 2.8 mm module. The mechanical diagram in Figure 2 illustrates the the top view of CM0, showing its shape, dimensions, external layout of key components (including SoC, radio module, and IPEX-1), and 132 pins. Pin numbering is arranged counter-clockwise from the top-left corner of CM0. Each pin is 0.6 mm wide and spaced 1 mm from neighbouring pins on the same edge.

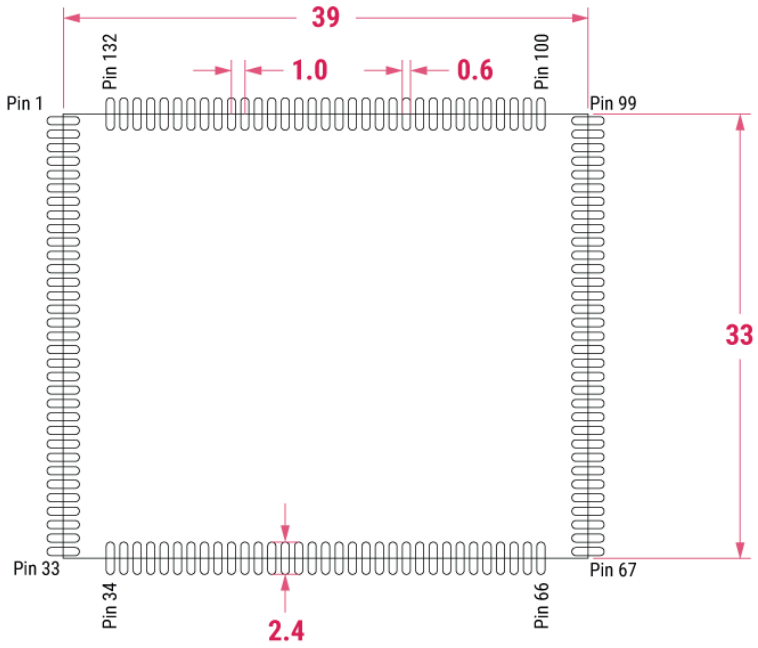
Figure 2.
Mechanical diagram of Compute Module Zero (CM0)



4.1.2. Recommended footprint

Figure 3 shows the recommended footprint specifications.

Figure 3.
Recommended footprint for Compute Module Zero (CM0)



4.2. Pinout

CM0 features 132 edge-plated castellated pins for mounting onto other boards. Table 5 provides a summary of each pin's assignment, including signal names and descriptions.

Table 5.
Pinout for the Compute Module Zero

Pin	Signal	Description
1	GND	Ground (0 V)
2	DSI_D3_P	DSI_D3_P
3	DSI_D3_N	DSI_D3_N
4	GND	Ground (0 V)
5	DSI_D2_P	DSI_D2_P
6	DSI_D2_N	DSI_D2_N
7	GND	Ground (0 V)
8	DSI_CK_P	DSI_CK_P
9	DSI_CLK_N	DSI_CK_N
10	GND	Ground (0 V)
11	DSI_D1_P	DSI_D1_P
12	DSI_D1_N	DSI_D1_N
13	GND	Ground (0 V)
14	DSI_D0_P	DSI_D0_P
15	DSI_D0_N	DSI_D0_N

Pin	Signal	Description
16	GND	Ground (0 V)
17	HDMI_HPD	Input HDMI hotplug; internally pulled down with a 100 kΩ. 5 V tolerant. Can be connected directly to a HDMI connector.
18	HDMI_SDA	Bidirectional HDMI SDA; internally pulled up with a 1.8 kΩ. 5 V tolerant; can be connected directly to a HDMI connector
19	HDMI_SCL	Bidirectional HDMI SCL; internally pulled up with a 1.8 kΩ. 5 V tolerant; can be connected directly to a HDMI connector
20	HDMI_CEC	Input HDMI CEC; internally pulled up with a 27 kΩ. 5 V tolerant; can be connected directly to a HDMI connector
21	GND	Ground (0 V)
22	HDMI_CK_N	Output HDMI clock negative
23	HDMI_CK_P	Output HDMI clock positive
24	GND	Ground (0 V)
25	HDMI_D0_N	Output HDMI TX0 negative
26	HDMI_D0_P	Output HDMI TX0 positive
27	GND	Ground (0 V)
28	HDMI_D1_N	Output HDMI TX1 negative
29	HDMI_D1_P	Output HDMI TX1 positive
30	GND	Ground (0 V)
31	HDMI_D2_N	Output HDMI TX2 negative
32	HDMI_D2_P	Output HDMI TX2 positive
33	GND	Ground (0 V)
34	GND	Ground (0 V)
35	USB_N	USB 2.0 D-
36	USB_P	USB 2.0 D+
37	GND	Ground (0 V)
38	USB_OTG	Input (3.3 V signal): USB OTG pin; internally pulled up; when grounded, CM0 becomes a USB host but the correct OS driver must also be used
39	CVBS	Composite video output
40	GND	Ground (0 V)
41	CM0_3.3V (Output)	3.3 V ± 5%. Power output max 300 mA per pin for a total of 600 mA; powered down when GLOBAL_EN set low
42	SDA0	I2C data pin (GPIO44): typically used for camera and display; internal 1.8 kΩ pull-up to CM0_3.3V
43	SCL0	I2C clock pin (GPIO45): typically used for camera and display; internal 1.8 kΩ pull-up to CM0_3.3V
44	CAM_GPIO	3.3 V signal: can be a GPIO (GPIO40)
45	GND	Ground (0 V)
46	CSI_D3_P	CSI_D3_P
47	CSI_D3_N	CSI_D3_N
48	GND	Ground (0 V)
49	CSI_D2_P	CSI_D2_P
50	CSI_D2_N	CSI_D2_N
51	GND	Ground (0 V)
52	CSI_CK_P	CSI_CK_P

Pin	Signal	Description
53	CSI_CK_N	CSI_CK_N
54	GND	Ground (0 V)
55	CSI_D1_P	CSI_D1_P
56	CSI_D1_N	CSI_D1_N
57	GND	Ground (0 V)
58	CSI_D0_P	CSI_D0_P
59	CSI_D0_N	CSI_D0_N
60	GND	Ground (0 V)
61	RUN_PG	Bidirectional pin. Can be driven low (via a 220 Ω resistor) to reset the CM0 CPU. As an output, a high signals that power is good and CPU is running. Internally pulled up to CM0_3.3V via 10 kΩ
62	GLOBAL_EN	Input; drive low to power off CM0 internally pulled up with a 10 kΩ to 5 V
63	GND	Ground (0 V)
64	CM0_1.8V (Output)	1.8 V ± 5%. Power output max 300 mA per pin for a total of 600 mA; powered down when GLOBAL_EN set low
65	CM0_1.8V (Output)	1.8 V ± 5%. Power output max 300 mA per pin for a total of 600 mA; powered down when GLOBAL_EN set low
66	GND	Ground (0 V)
67	5V (Input)	4.75 V to 5.25 V main power input
68	5V (Input)	4.75 V to 5.25 V main power input
69	GND	Ground (0 V)
70	NC	Do not connect to anything
71	NC	Do not connect to anything
72	GND	Ground (0 V)
73	GPIO21	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
74	GPIO20	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
75	GND	Ground (0 V)
76	GPIO26	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
77	GPIO16	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
78	GND	Ground (0 V)
79	GPIO19	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
80	GPIO13	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
81	GND	Ground (0 V)
82	GPIO12	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
83	GPIO6	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
84	GND	Ground (0 V)
85	GPIO5	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
86	ID_SC	(RP1 GPIO 1) GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
87	GND	Ground (0 V)
88	ID_SD	(RP1 GPIO 0) GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
89	GPIO7	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
90	GND	Ground (0 V)

Pin	Signal	Description
91	GPIO8	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
92	GPIO11	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
93	GND	Ground (0 V)
94	GPIO25	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
95	GPIO9	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
96	GND	Ground (0 V)
97	GPIO10	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
98	GPIO24	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
99	GND	Ground (0 V)
100	GND	Ground (0 V)
101	GPIO23	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
102	GPIO22	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
103	GND	Ground (0 V)
104	GPIO27	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
105	GPIO18	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
106	GND	Ground (0 V)
107	GPIO17	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
108	GPIO15	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
109	GND	Ground (0 V)
110	GPIO14	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
111	GPIO4	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V
112	GND	Ground (0 V)
113	GPIO3	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V ; internal 1.8 kΩ pull-up to GPIO_VREF
114	GPIO2	GPIO: typically a 3.3 V signal, but can be a 1.8 V signal by connecting GPIO_VREF to CM0_1.8V ; internal 1.8 kΩ pull-up to GPIO_VREF
115	GND	Ground (0 V)
116	WiFi_ON	Can be left floating; if driven low, the Wi-Fi interface will be disabled. Internally pulled up through 10 kΩ to CM0_3.3V
117	BT_ON	Can be left floating; if driven low, the Bluetooth interface will be disabled; internally pulled up through 10 kΩ to CM0_3.3V
118	LED_nACT	Active-low Pi activity LED; 5 mA max; this signal drives typically drives an activity LED
119	CM0_3.3V (Output)	3.3 V ± 5%. Power output max 300 mA per pin for a total of 600 mA; powered down when GLOBAL_EN set low
120	CM0_3.3V (Output)	3.3 V ± 5%. Power output max 300 mA per pin for a total of 600 mA; powered down when GLOBAL_EN set low
121	nRPI_BOOT	A low on this pin forces booting from an RPI server (for example, PC or a Raspberry Pi); if not used, leave floating; internally pulled up through 10 kΩ to CM0_3.3V
122	SD_VREF	Must be connected to CM0_3.3V (pins 119 and 120) for 3.3 V SD_CLK , SD_CMD and SD_DAT0-3 or CM0_1.8V (pins 64 and 65) for 1.8 V SD_CLK , SD_CMD and SD_DAT0-3 ; this pin can't be floating or connected to ground
123	GND	Ground (0 V)
124	SD_DAT1	SD card/eMMC Data1 signal (only available on CM0Lite)
125	SD_DAT0	SD card/eMMC Data0 signal (only available on CM0Lite)

Pin	Signal	Description
126	GND	Ground (0 V)
127	SD_CLK	SD card clock signal (only available on CM0Lite)
128	SD_CMD	SD card/eMMC Command signal (only available on CM0Lite)
129	GND	Ground (0 V)
130	SD_DAT3	SD card/eMMC Data3 signal (only available on CM0Lite)
131	SD_DAT2	SD card/eMMC Data2 signal (only available on CM0Lite)
132	GND	Ground (0 V)

4.2.1. Pin guidelines

The following instructions provide guidance for grounding, connector usage, voltage limits, and power rail considerations, and precautions against improper voltage application.

- **Grounding.** Always connect all ground pins.
- **GPIO voltage limits.** GPIO pins 0 to 27 are the same as the 40-pin connector on Raspberry Pi 5. Depending on your signalling, their voltage must not exceed:
  - 3.3 V (`CM0_3.3V`) when using 3.3 V signalling.
  - 1.8 V (`CM0_1.8V`) when using 1.8 V signalling.
- **Power rails.** If you use power rails `CM0_3.3V` or `CM0_1.8V` to supply devices other than the GPIO reference voltage (`GPIO_VREF`), you must design for safe behaviour during unexpected power loss (for example, the 5 V line falls below 4.5 V):
  - If you use the 1.8 V rail (`CM0_1.8V`), ensure that the current draw goes down to zero (no load) if power suddenly drops.
  - If you use the 3.3 V rail (`CM0_3.3V`), ensure that the 3.3 V rail voltage never falls below the 1.8 V rail voltage if power suddenly drops. The 3.3 V rail voltage usually stays above the 1.8 V rail voltage during power-down, but verify your design. If the 3.3 V rail does fall below 1.8 V, add circuitry to disconnect 3.3 V devices to prevent damage.
- **Reverse voltage.** Don't apply reverse voltage on any pin. This means that when CM0 is powered-down or off, there must be no external voltage applied to any pin, otherwise CM0 might not power up again.

4.2.2. Differential pairs

We recommend that positive and negative (P/N) signals within a differential pair are length-matched to within 0.15 mm. Depending on the interface, the matching tolerance can be more relaxed between different pairs. For example, HDMI pair-to-pair matching can typically be within 25 mm, so no extra matching is required on a typical board.

100 Ω differential pair signal lengths

All 100 Ω differential pairs on CM0 are length-matched to less than 0.1 mm for P/N signals. We recommend that pairs are also matched on the interface board. On CM0, pair-to-pair length matching isn't always maintained because many interfaces don't require precise matching between different pairs.

90 Ω differential pair signal lengths

All 90 Ω differential pair on CM0 (USB pair) are length-matched to less than 0.1 mm for P/N signals.

4.3. Electrical specifications

For safe and reliable operation of CM0, observe the following electrical parameters and limitations.

4.3.1. Absolute maximum ratings

Warning

Stresses above those listed in Table 6 can cause permanent damage to the device. This is a stress rating only; functional operation of the device under these or any other conditions above those listed in the operational sections of this specification isn't implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Table 6 lists the absolute maximum ratings for key voltage parameters on the CM0. These values represent the limits beyond which damage to the device can occur and shouldn't be exceeded.

Table 6.
Absolute maximum ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{IN}	5 V input voltage	−0.5	6.0	V
V_{GPIO_VREF}	GPIO voltage	−0.5	3.6	V
V_{gpio}	GPIO input voltage	−0.5	V_{GPIO_VREF} + 0.5	V

Note

V_{GPIO_VREF} is the GPIO bank voltage, which must be tied to either `CM0_3.3V` or `CM0_1.8V` .

4.3.2. DC characteristics

Table 7 details the DC electrical characteristics of the GPIO pins on CM0. It describes how the GPIO pins perform under different conditions (such as different reference voltages) and provides the expected ranges for each parameter (minimum, typical, and maximum values).

Table 7.
DC characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{IL(gpio)}$	Input low voltage	V_{GPIO_VREF} = 3.3 V	0	-	0.8	V
$V_{IH(gpio)}$	Input high voltage	V_{GPIO_VREF} = 3.3 V	2.0	-	V_{GPIO_VREF}	V
$V_{IL(gpio)}$	Input low voltage	V_{GPIO_VREF} = 1.8 V	0	-	0.35*V_{GPIO_VREF}	V
$V_{IH(gpio)}$	Input high voltage	V_{GPIO_VREF} = 1.8 V	0.65*V_{GPIO_VREF}	-	V_{GPIO_VREF}	V
$I_{IL(gpio)}$	Input leakage current	V_{GPIO_VREF} = 3.3 V	-	-	5	µA
$I_{IL(gpio)}$	Input leakage current	V_{GPIO_VREF} = 1.8 V	-	-	5	µA
$V_{OL(gpio)}$	Output low voltage	-	-	-	0.4	V
$V_{OH(gpio)}$	Output high voltage	V_{GPIO_VREF} = 3.3 V	V_{GPIO_VREF} - 0.4	-	-	V
$V_{OH(gpio)}$	Output high voltage	V_{GPIO_VREF} = 1.8 V	V_{GPIO_VREF} - 0.4	-	-	V
$I_{OL(gpio)}$	Output low current	16 mA, V_{GPIO_VREF} = 3.3 V	18	-	-	mA
$I_{OH(gpio)}$	Output high current	16 mA, V_{GPIO_VREF} = 3.3 V	17	-	-	mA
$I_{OL(gpio)}$	Output low current	16 mA, V_{GPIO_VREF} = 1.8 V	12	-	-	mA
$I_{OH(gpio)}$	Output high current	16 mA, V_{GPIO_VREF} = 1.8 V	10	-	-	mA
$R_{PU(gpio)}$	Pull-up resistor		50	-	65	kΩ
$R_{PD(gpio)}$	Pull-down resistor		50	-	65	kΩ

4.3.3. Current consumption

Table 8 presents key current consumption characteristics for CM0 under various operating conditions. It details the typical shutdown, idle, and operational currents measured with different input voltages and control signals. Actual figures greatly depend on the end application.

Table 8.

Current consumption characteristics for Compute Module Zero (CM0)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$I_{shutdown}$	Shutdown current	`GLOBAL_EN` < 0.4 V	-	0.5	-	mA
I_{idle}	Idle current	`GLOBAL_EN` > 2 V	-	250	-	mA
I_{load}	Operation current	`GLOBAL_EN` > 2 V	-	670	-	mA

4.4. Thermal characteristics

The BCM2837 SoC on CM0 has built-in thermal management that reduces its clock speed to keep the SoC temperature below 85°C. To avoid overheating, the SoC might automatically throttle its performance in high ambient temperatures. If the SoC can't reduce its temperature enough through throttling, its case temperature can exceed 85°C. Any thermal management solution must ensure that the ambient temperatures of the other silicon components on the board stay within their safe operating range.

CM0's overall operating temperature range is from –20°C to +85°C (non-condensing). Wireless RF performance is best within –20°C to +75°C.

4.5. Mean time between failure (MTBF)

Mean time between failure (MTBF) measures how long, on average, each device is expected to operate before failure. Table 9 shows the MTBF for CM0, which varies depending on environmental conditions. MTBF is not shown for CM0Lite.

Table 9.

Mean time between failure (MTBF) for Compute Module Zero (CM0)

Environment	Description	CM0 MTBF
Ground, benign	A stable, non-mobile environment where temperature and humidity are controlled, such as laboratories, business and scientific computer complexes, and medical equipment rooms. In these environments, devices generally last longer.	374000 hours
Ground, mobile	A high-stress environment with vibration, temperature swings, humidity variations, and frequent movement, such as equipment in vehicles and handheld communication devices. In these environments, life expectancy drops.	32000 hours

5. Troubleshooting

CM0 requires stable power to start up. It has a number of power-up and boot stages before it starts. If an error occurs at any of these stages, CM0 might fail to start or run as expected. The following steps help you to diagnose and resolve the issue by checking hardware power rails and signals for proper voltages and load behaviour:

1. **Test the 5 V supply under load:** Pull `GLOBAL_EN` low and apply an external 0.5 A load to the 5 V supply. The voltage should remain above 4.75 V (including noise), ideally, staying above 4.9 V.
2. **Check `GLOBAL_EN` goes high:** Remove the pull-down on `GLOBAL_EN` and then check that `GLOBAL_EN` now goes high; measure the voltage on this pin or check its logic state to confirm it goes high.
3. **Confirm that the voltage rails rise correctly:**
    - Check the 3.3 V supply rises to more than 3.15 V. If it doesn't, this suggests there is too much load on the 3.3 V rail.
    - Check the 1.8 V supply rises to more than 1.71 V. If it doesn't, this suggests there is too much load on the 1.8 V rail.
4. **Check `RUN_PG` goes high:** Measure the voltage on the pin and check that it's above 3.15 V.
5. **Check the activity LED (`LED_nACT`) to verify the boot process:** The LED should oscillate to indicate booting; check it isn't flashing an error code. To decode error code patterns, see the Raspberry Pi documentation.

We also recommend avoiding known issues by ensuring the system software (firmware and kernel) are up to date. Keeping your firmware up to date can resolve many system issues and improve stability because newer versions contain improvements to the system. Similarly, new kernel releases often include important security patches and performance improvements.

6. Ordering information

CM0 comes in a range of variants distinguished by wireless capability and eMMC storage capacity. Each CM0 variant is identified by a unique order code (part number).

6.1. Order quantity and packaging

You can order a specific number of one or more CM0 devices that will arrive individually boxed, or you can make a bulk order that will come in a single shipper. Small quantities supplied in individual cardboard boxes have an internal ESD coating so that a separate ESD bag isn't required. This packaging is recyclable to reduce waste.

6.2. Part number codes

Table 10 explains the structure of part numbers for CM0 variants. It details how the model, wireless capability, RAM size, and eMMC storage capacity are encoded within the part number.

Table 10.
Part number information for Compute Module Zero (CM0)

Model	Wireless	RAM LPDDR2	eMMC storage
CM0	0 = No	00 = 512 MB	000 = 0 GB (Lite)
	1 = Yes		008 = 8 GB
			016 = 16 GB
Example part number			
CM0	1	00	016

6.3. Product variants

Table 11 shows available variants for CM0 by part number, detailing wireless support, RAM size, eMMC storage capacity and RPL numbers. Other configurations can be custom ordered.

Table 11.
Available product variants for Compute Module Zero (CM0), including CM0Lite

Part number	Wireless	RAM LPDDR2	Storage eMMC	RPL number
CM0000000	-	512 MB	Lite (0 GB)	SC2230
CM0000008	-	512 MB	8 GB	SC2231
CM0000016	-	512 MB	16 GB	SC2232
CM0100000	Yes	512 MB	Lite (0 GB)	SC2233
CM0100008	Yes	512 MB	8 GB	SC2234
CM0100016	Yes	512 MB	16 GB	SC2235

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